Anti-collision flowchart

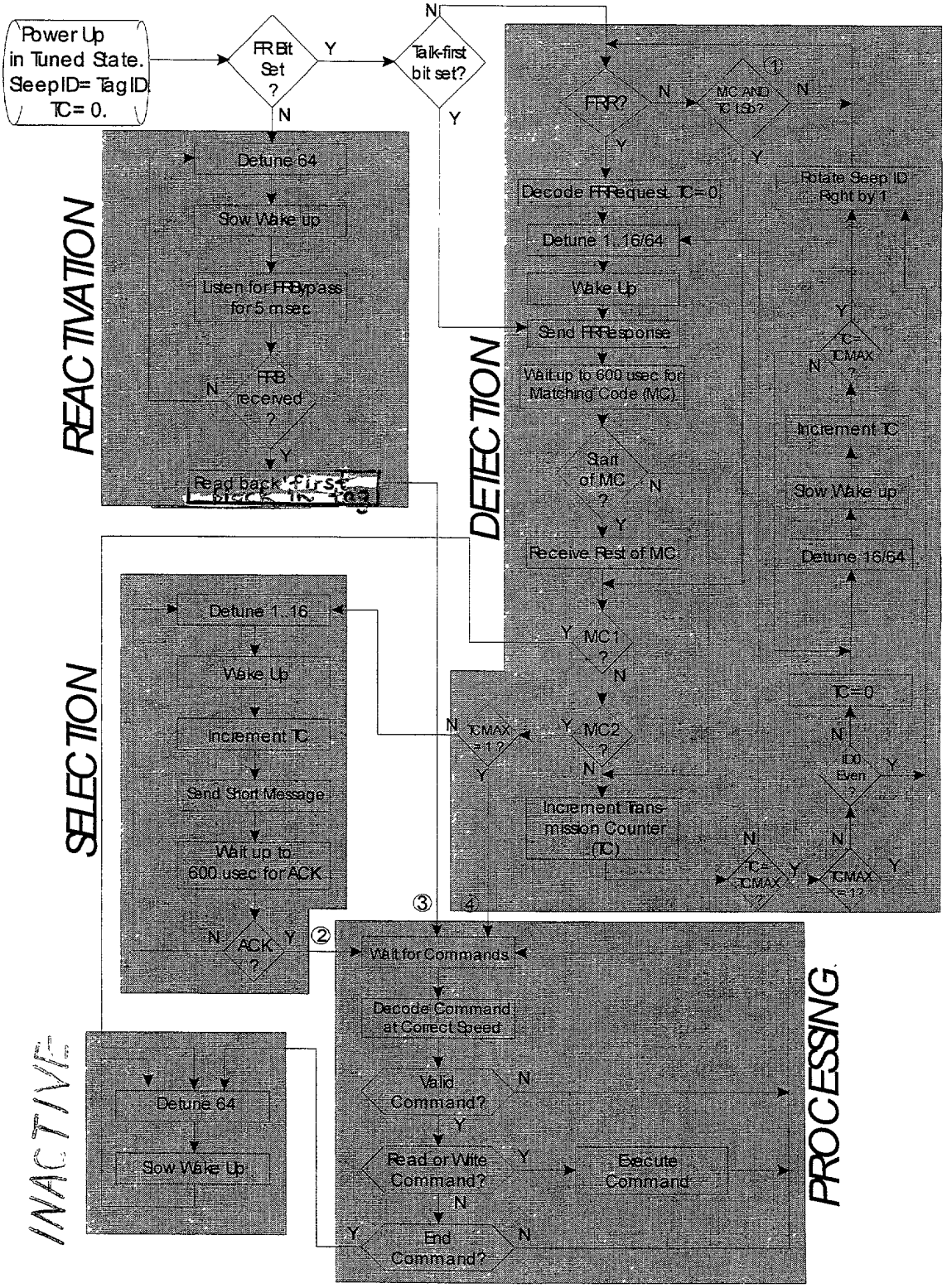


FIG. 1

FIG 2

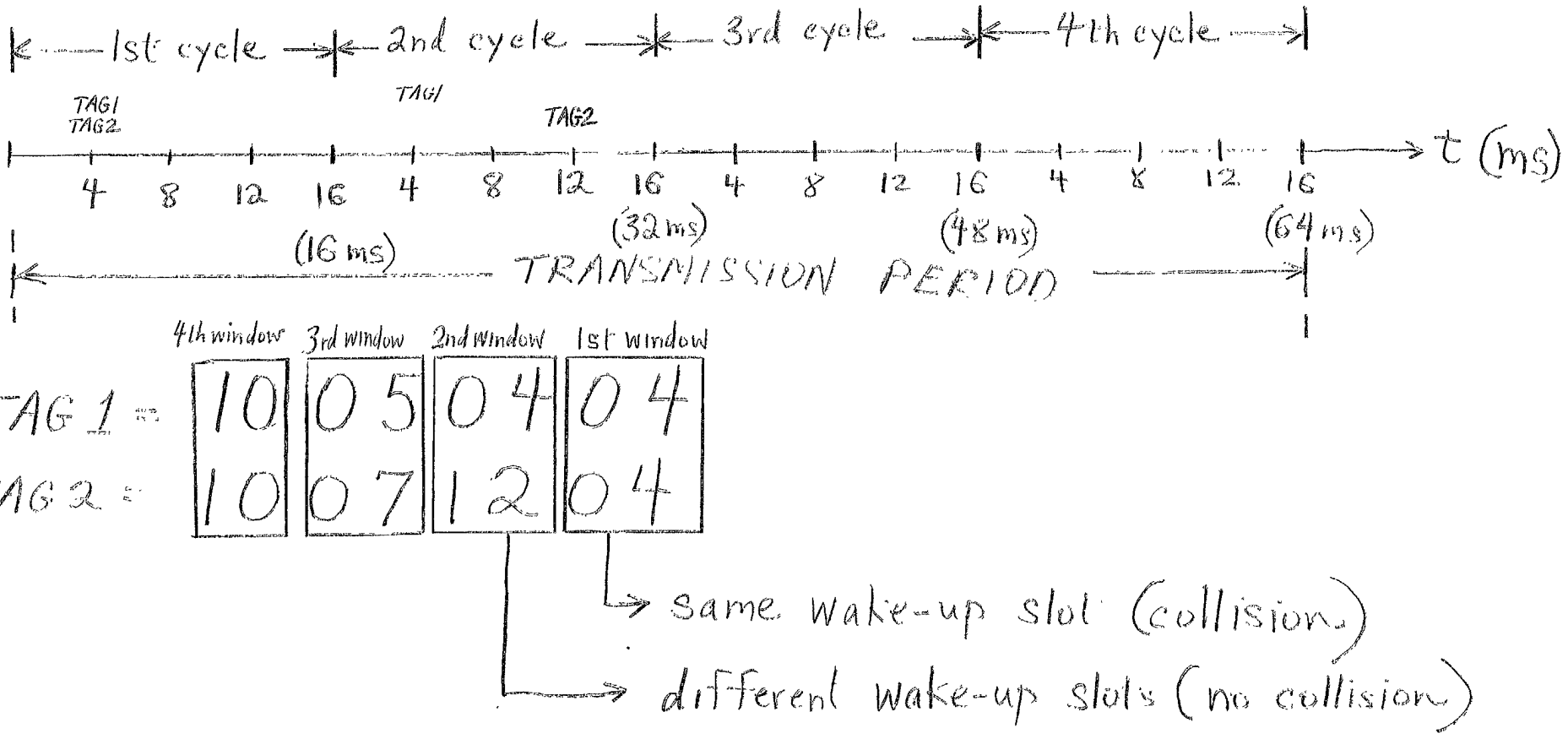
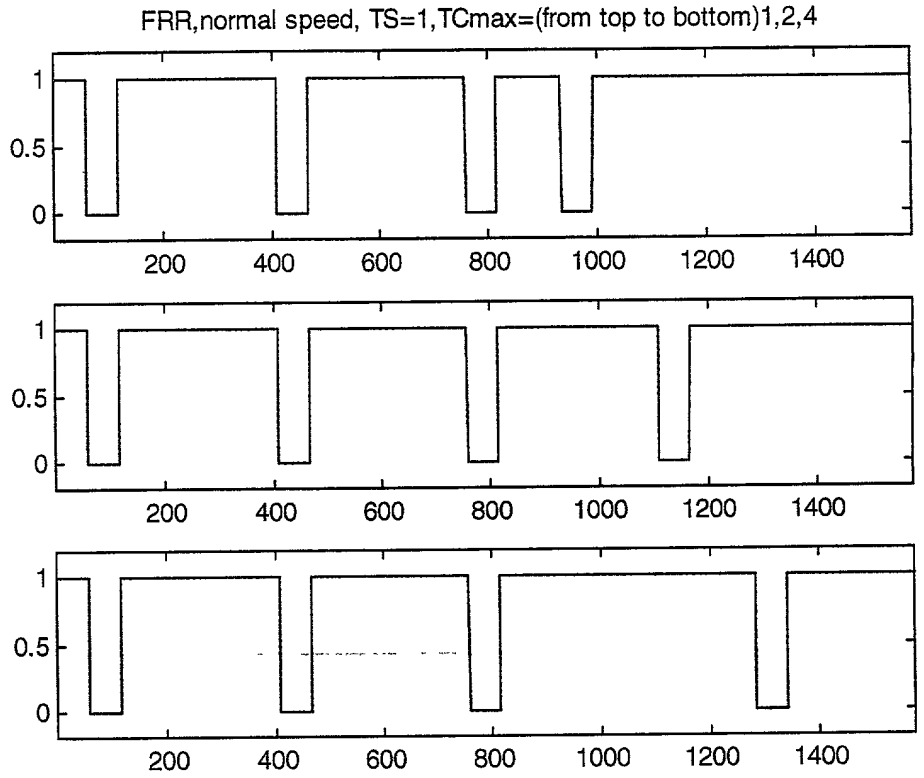

1st cycle
2nd cycle
3rd cycle
4th cycle
TAG1
TAG2
TAG1
TAG2
4 8 12 16 4 8 12 16 4 8 12 16 4 8 12 16
t (ms)
(16 ms)
(32 ms)
(48 ms)
(64 ms)
TRANSMISSION PERIOD
4th window
3rd window
2nd window
1st window
TAG 1 =
10 05 04 04
TAG 2 =
10 07 12 04
same wake-up slot (collision)
different wake-up slots (no collision)

FIG. 3A


FRR,normal speed, TS=1,TCmax=(from top to bottom)1,2,4
1
0.5
0
200
400
600
800
1000
1200
1400

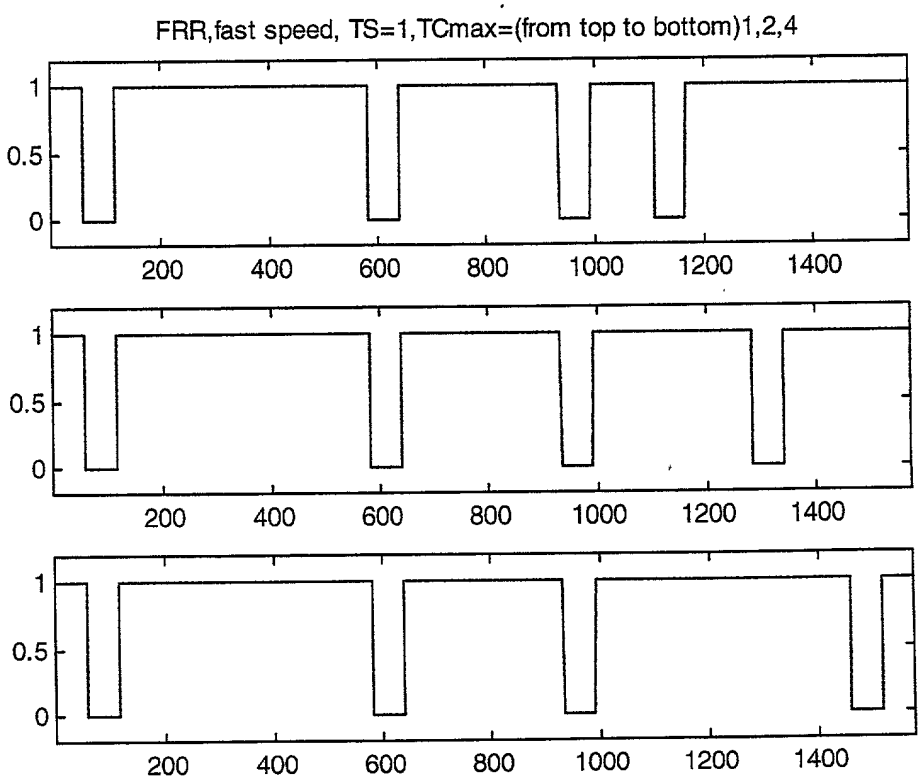
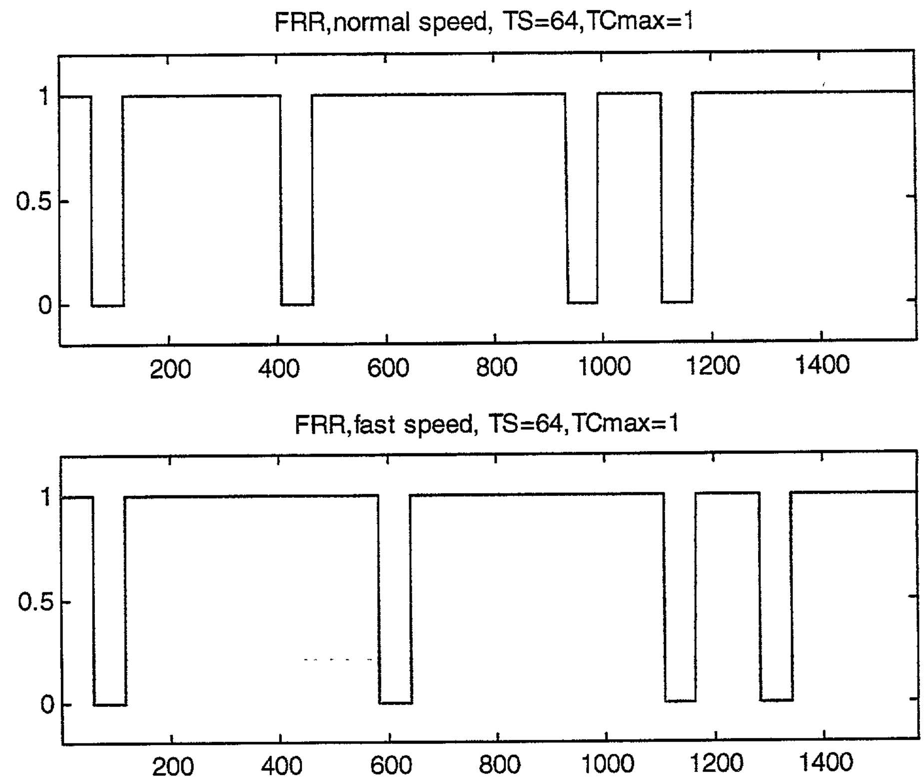

FRR,fast speed, TS=1,TCmax=(from top to bottom)1,2,4
1
0.5
0
200
400
600
800
1000
1200
1400

FIG. 3B


FRR,normal speed, TS=64,TCmax=1
FRR,fast speed, TS=64,TCmax=1
1
0.5
0
200
400
600
800
1000
1200
1400

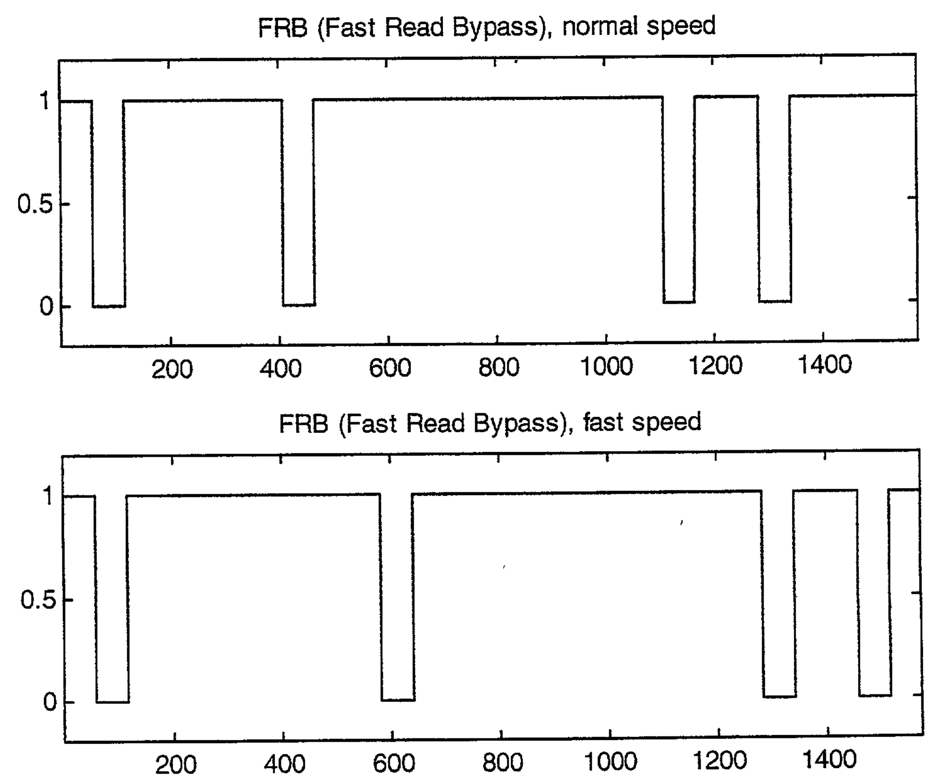

FRB (Fast Read Bypass), normal speed
FRB (Fast Read Bypass), fast speed
1
0.5
0
200
400
600
800
1000
1200
1400

FIG. 3C

"Match" code = Tag ID bit range a:b
[4(TC+1)+3]modulo32:[4TC]modulo32

FIG. 4

Example : Tag ID =$825FE1A0

TC	"Match"	ACK
0	$A0	$1
1	$1A	$E
2	$E1	$F
3	$FE	$5
4	$5F	$2
5	$25	$8
6	$82	$0
7	$08	$A

FIG. 5

Acknowledge = Tag ID bit range a:b
[4(TC+2)+3]modulo32:[4TC+8]modulo32

FIG. 6

Timeslots	Wake-up slot = Tag ID bit range a:b
16	[[4(TC+1)-1]modulo32: [4TC]modulo32] XOR TC LSb
64	[[4(TC+1)+1]modulo32: [4TC]modulo32] XOR TC LSb

FIG. 7

Example: Tag ID $825FE1A0

TC	Relevant Number		Sleep Time 16		Sleep Time 64		Sleep Time 16 semi-inv.		Sleep Time 64 semi-inv.	
Tag ID $825FE1A0							Wake-up slot			
0	$A0	b1010 0000	$0	0	$20	32	$0	0	$20	32
1	$1A	b0001 1010	$A	10	$1A	26	**$5**	**5**	**$25**	**37**
2	$E1	b1110 0001	$1	1	$21	33	$1	1	$21	33
3	$FE	b1111 1110	$E	14	$3E	62	**$1**	**1**	**$01**	**1**
4	$5F	b0101 1111	$F	15	$1F	31	$F	15	$1F	31
5	$25	b0010 0101	$5	5	$25	37	**$A**	**10**	**$1A**	**26**
6	$82	b1000 0010	$2	2	$02	2	$2	2	$02	2
7	$08	b0000 1000	$8	8	$08	8	**$7**	**7**	**$37**	**55**

FIG. 8